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- 1 [Optimization: High-speed, scalable, real-time simulation using DSP arrays](#)  
 Roy Crosbie, John Zenor, Richard Bednar, Dale Word, Narain Hingorani, Terry Ericson  
 May 2004 **Proceedings of the eighteenth workshop on Parallel and distributed simulation**

 Full text available: [pdf\(156.87 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#)

Real-time simulation is a familiar technique for testing hardware and software in the loop and for operator training. An important parameter of these simulations is the frame-time necessary to capture the dynamics of the system being simulated. Modern power electronic systems, using higher frequency pulse-width modulation (PWM) converter control demand frame times that are significantly shorter than those found in most real-time simulators. The paper describes an approach to real-time simulation ...

- 2 [Electroid-oriented adiabatic switching circuits](#)  
 David J. Frank, Paul M. Solomon  
 April 1995 **Proceedings of the 1995 international symposium on Low power design**

 Full text available: [pdf\(271.92 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

- 3 [Flow diagrams, turing machines and languages with only two formation rules](#)  
 Corrado Böhm, Giuseppe Jacopini  
 May 1966 **Communications of the ACM**, Volume 9 Issue 5

 Full text available: [pdf\(630.89 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#)

- 4 [Tradeoffs and design of an ultra low power UHF transceiver integrated in a standard digital CMOS process](#)  
 Alain-Serge Porret, Thierry Melly, E. A. Vittoz, C. C. Enz  
 August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

 Full text available: [pdf\(1.17 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A broad range of high-volume consumer applications require low-power, battery operated, wireless microsystems and sensors. These systems should conciliate a sufficient battery lifetime with reduced dimensions, low cost and versatility. The design of such systems highlights many tradeoffs between performances, lifetime, cost and power consumption.


Also, special circuit and design techniques are needed to comply with the reduced supply voltage (down to 1V). These considerations are ...

**Keywords:** CMOS, RF, low-power, low-voltage, transceiver

##### 5 Signal processing in SETI

D. K. Cullers, Ivan R. Linscott, Bernard M. Oliver

November 1985 **Communications of the ACM**, Volume 28 Issue 11

Full text available:  pdf(3.96 MB)


Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

The Search for Extraterrestrial Intelligence (SETI), now being planned at NASA, will require a prodigious amount of highly concurrent signal processing to be done in real time by special-purpose hardware.

##### 6 Elastically deformable models

Demetri Terzopoulos, John Platt, Alan Barr, Kurt Fleischer

August 1987 **ACM SIGGRAPH Computer Graphics , Proceedings of the 14th annual conference on Computer graphics and interactive techniques**, Volume 21 Issue 4

Full text available:  pdf(4.88 MB)


Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The theory of elasticity describes deformable materials such as rubber, cloth, paper, and flexible metals. We employ elasticity theory to construct differential equations that model the behavior of non-rigid curves, surfaces, and solids as a function of time. Elastically deformable models are active: they respond in a natural way to applied forces, constraints, ambient media, and impenetrable obstacles. The models are fundamentally dynamic and realistic animation is created by numerically solving ...

##### 7 Scalable lock-free dynamic memory allocation

Maged M. Michael

June 2004 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2004 conference on Programming language design and implementation**, Volume 39 Issue 6

Full text available:  pdf(213.94 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


Dynamic memory allocators (malloc/free) rely on mutual exclusion locks for protecting the consistency of their shared data structures under multithreading. The use of locking has many disadvantages with respect to performance, availability, robustness, and programming flexibility. A lock-free memory allocator guarantees progress regardless of whether some threads are delayed or even killed and regardless of scheduling policies. This paper presents a completely lock-free memory allocator. It uses ...

**Keywords:** async-signal-safe, availability, lock-free, malloc

##### 8 An asynchronous protocol for distributed computation of RSA inverses and its applications

Christian Cachin

July 2003 **Proceedings of the twenty-second annual symposium on Principles of distributed computing**

Full text available:  pdf(1.19 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents an efficient asynchronous protocol to compute RSA inverses with respect to a public RSA modulus  $N$  whose factorization is secret and shared among a group

of parties. Given two numbers  $x$  and  $e$ , the protocol computes  $y$  such that  $y^e \equiv x \pmod{N}$ . A synchronous protocol for this task has been presented by Catalano, Gennaro, and Halevi (Eurocrypt 2000), but the standard approach for turning this into an asynchronous protocol would re ...

**Keywords:** Byzantine agreement, Cryptography, threshold signatures, verifiable random functions, verifiable secret sharing

9 Biological applications: A hybrid genetic algorithm with pattern search for finding heavy atoms in protein crystals 

Joshua L. Payne, Margaret J. Eppstein

June 2005 **Proceedings of the 2005 conference on Genetic and evolutionary computation GECCO '05**

Full text available:  pdf(317.54 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


One approach for determining the molecular structure of proteins is a technique called isomorphous replacement, in which crystallographers dope protein crystals with heavy atoms, such as mercury or platinum. By comparing measured amplitudes of diffracted x-rays through protein crystals with and without the heavy atoms, the locations of the heavy atoms can be estimated. Once the locations of the heavy atoms are known, the phases of the diffracted x-rays through the protein crystal can be estimat ...

**Keywords:** crystallographic phasing, crystallography, genetic algorithms, heavy atom method, hybrid evolutionary algorithms, isomorphous replacement, pattern search, phase problem

10 Jump PDA's, deterministic context-free languages principal AFDLs and polynomial time recognition—(Extended Abstract) 

Sheila A. Greibach

April 1973 **Proceedings of the fifth annual ACM symposium on Theory of computing**

Full text available:  pdf(636.59 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Every deterministic context-free language can be accepted by a deterministic finite delay pda with jumps. Increasing the number of types or occurrences of jumps increases the family of languages accepted with finite delay. Hence the family of deterministic context-free language is a principal AFDL; there is a context-free language  $L_0$  such that every context-free language is an inverse gsm image of  $L_0$  or  $L_0 - \{e\}$ . A si ...

11 CONCERT: a concurrent transient fault simulator for nonlinear analog circuits 

Junwei Hou, Abhijit Chatterjee

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(861.89 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

12 A programmer's description of L6 

Kenneth C. Knowlton

August 1966 **Communications of the ACM**, Volume 9 Issue 8

Full text available:  pdf(845.56 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


Bell Telephone Laboratories' Low-Level Linked List Language L6 (pronounced "L-six") is a new programming language for list structure manipulations. It contains many of the

facilities which underlie such list processors as IPL, LISP, COMIT and SNOBOL, but permits the user to get much closer to machine code in order to write faster-running programs, to use storage more efficiently and to build a wider variety of linked data st ...

### 13 Cryptographic limitations on learning Boolean formulae and finite automata

Michael Kearns, Leslie Valiant

January 1994 **Journal of the ACM (JACM)**, Volume 41 Issue 1

Full text available:  [pdf\(2.26 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we prove the intractability of learning several classes of Boolean functions in the distribution-free model (also called the Probably Approximately Correct or PAC model) of learning from examples. These results are representation independent, in that they hold regardless of the syntactic form in which the learner chooses to represent its hypotheses. Our methods reduce the problems of cracking a number of well-known public-key cryptosystems to the l ...

### 14 Estimation of the defective IDDQ caused by shorts in deep-submicron CMOS ICs

R. Rodríguez-Montanés, J. Figueras

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:  [pdf\(222.23 KB\)](#)

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The defective IDDQ in deep-submicron full complementary MOS circuits with shorts is estimated. High performance and also low power scenarios are considered. The technology scaling, including geometry reductions of the transistor dimensions, power supply voltage reduction, carrier mobility degradation and velocity saturation, is modeled. By means of the characterization of the saturation current of a simple MOSFET, a lower bound of IDDQ defective consumption versus Leff is found. Quiescent current ...


**Keywords:** IDDQ testability, deep-submicron, CMOS

### 15 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Full text available:  [pdf\(613.63 KB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

 [html\(2.78 KB\)](#)

### 16 Fraction-free algorithms for linear and polynomial equations

George C. Nakos, Peter R. Turner, Robert M. Williams

September 1997 **ACM SIGSAM Bulletin**, Volume 31 Issue 3

Full text available:  [pdf\(790.20 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

This paper extends the ideas behind Bareiss's fraction-free Gauss elimination algorithm in a number of directions. First, in the realm of linear algebra, algorithms are presented for fraction-free LU "factorization" of a matrix and for fraction-free algorithms for both forward and back substitution. These algorithms are valid not just for integer computation but also for any matrix system where the entries are taken from a unique factorization domain such as a polynomial ring. The second part of ...

### 17 Multiresolution green's function methods for interactive simulation of large-scale elastostatic objects

Doug L. James, Dinesh K. Pai

January 2003 **ACM Transactions on Graphics (TOG)**, Volume 22 Issue 1

Full text available:  [pdf\(8.69 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present a framework for low-latency interactive simulation of linear elastostatic models, and other systems arising from linear elliptic partial differential equations, which makes it feasible to interactively simulate large-scale physical models. The deformation of the models is described using precomputed Green's functions (GFs), and runtime boundary value problems (BVPs) are solved using existing Capacitance Matrix Algorithms (CMAs). Multiresolution techniques are introduced to control the ...

**Keywords:** Capacitance matrix, Green's function, deformation, elastostatic, fast summation, force feedback, interactive real-time applications, lifting scheme, real-time, updating, wavelets

18 Research session 4: data integration & interoperability: Composition of mappings given by embedded dependencies 

Alan Nash, Philip A. Bernstein, Sergey Melnik

June 2005 **Proceedings of the twenty-fourth ACM SIGMOD-SIGACT-SIGART symposium on Principles of database systems**

Full text available:  [pdf\(198.18 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#)

Composition of mappings between schemas is essential to support schema evolution, data exchange, data integration, and other data management tasks. In many applications, mappings are given by embedded dependencies. In this paper, we study the issues involved in composing such mappings.

19 Session S8.2: system synthesis: HW / SW partitioning approach for reconfigurable system design 

K. Ben Chehida, M. Auguin

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available:  [pdf\(520.12 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents a Genetic Algorithm (GA) based approach for Hardware/Software partitioning targeting an architecture composed of a processor and a dynamically reconfigurable datapath (FPGA). From an acyclic task graph and a set of Area-Time implementation trade off points for each task, our GA performs HW/SW partitioning and scheduling such that the global application execution time is minimized. The efficiency of our GA is established through its application to an AC-3 decoder function and ...

**Keywords:** HW/SW partitioning, clustering, codesign, dynamic reconfiguration, genetic algorithm

20 Principles and realization strategies of multilevel transaction management 

Gerhard Weikum

March 1991 **ACM Transactions on Database Systems (TODS)**, Volume 16 Issue 1

Full text available:  [pdf\(3.72 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

One of the demands of database system transaction management is to achieve a high degree of concurrency by taking into consideration the semantics of high-level operations. On the other hand, the implementation of such operations must pay attention to conflicts on the storage representation levels below. To meet these requirements in a layered

architecture, we propose a multilevel transaction management utilizing layer-specific semantics. Based on the theoretical notion of multilevel serial ...

**Keywords:** atomicity persistence concurrency control, multilevel transactions, persistence, serializability

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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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